Deep-Level Transient Spectroscopy

Part 3 Laboratories

October 7, 2004

Contents

1 Introduction **2**

2 Elementary Semiconductor Physics **2**

3 Background: Electrical Analysis of Semiconductors **3**

3.1 Schottky Barrier Diodes . . . 3

3.2 Deep Level Transient Spectroscopy (DLTS) . . . 5

3.2.1 The capacitance transient and DLTS signal . . . 6

3.2.2 Calculating trap energy levels and capture cross-sections . . . 7

3.2.3 Calculating trap concentrations . . . 8

3.3 Deep-level traps in implanted silicon . . . 9

4 Experimental Work **9**

4.1 The racks of electronics . . . 10

4.2 The computer stuff . . . 10

4.3 The cryostat and sample holder . . . 11

4.4 Making a room temperature C-V measurement . . . 12

4.5 Making a low temperature C-V measurement . . . 13

4.6 Analysing the C-V data . . . 14

4.6.1 Determine the built-in voltage of the diode . . . 14

4.6.2 Calculate the barrier height . . . 14

4.6.3 Calculate the active dopant concentration . . . 14

4.7 DLTS measurement . . . 15

4.8 Perfoming a C-T measurement . . . 17

4.9 Analysing the DLTS data . . . 17

4.9.1 Calculate the defect concentrations . . . 17

4.9.2 Characterise the defects observed . . . 17

4.10 If time permits.. . . . 18

1 Introduction

Semiconductor devices have revolutionised the world in which we live and have become such a part of our everyday lives that we often take it for granted that they can and will perform the task that they were designed for. However, due to their high quality the single crystal semiconductors wafers used are in fact extremely sensitive to defects created arising from contamination from impurities and bombardment from high energy ions.

In this experiment you will examine how the static and transient capacitance of a metal-semiconductor diode (Schottky diode) varies with applied bias, temperature and time using Capacitance-Voltage (C-V) measurements and Deep-Level Transient Spectroscopy (DLTS). These techniques are routinely used for wafer characterisation by the semiconductor industry. DLTS is one of the most sensitive techniques available with the ability to measure defect concentrations down to 1 defect per 10^{10} silicon atoms. (Wow!)

Analysing semiconductors (eg. Silicon wafers) using Deep Level Transient Spectroscopy (DLTS) reveals vital information about the nature and effect of defects present in the semiconductor. DLTS is one of the few techniques that probes the traps in the band-gap introduced by ion implantation of dopants.

The experiment involves analysing a Silicon wafer which has been irradiated or implanted with a low dose of ions, and characterising the resulting defects. The sample is cooled with liquid nitrogen, a metal contact is deposited to form a Schottky diode, and the capacitance measured under a variety of voltage pulses and temperatures. Students will have the opportunity to gain a deeper understanding of semiconductor diodes and the band-structure description of semiconductors. From the analysis of the results you will be able to determine the nature and extent of radiation damage that the silicon chip has been exposed to. In understanding the techniques applied you will gain a deeper understanding of semiconductor diodes and the band-structure description of semiconductors.

2 Elementary Semiconductor Physics

The sections that follow assume a working knowledge of elementary semiconductor physics, in particular band diagrams and doping. Some of you will be comfortable with these concepts because you have met them in other courses, but others may me meeting them for the first time. A good introduction is given in Streetman, a photocopy of which can be found in the lab. Also feel free to ask your demonstrators any questions, no matter how dumb they sound (either the questions or the demonstrators :-).

Here is a list of jargon words, the meaning of which you need to know in order to understand the rest of the prac notes:

- Semiconductor
- n-type
- p-type
- Work Function
- Fermi Level
- Capacitance
- Effective mass
- Diode
- Rectify
- Energy Band (Conduction band, valence band)
- Band gap
- Band Bending

- Dopant
- Depletion region
- Energy Level
- Deep level
- Majority carrier
- Minority carrier
- Carrier concentration
- Trap
- Capture cross-section
- Defect

3 Background: Electrical Analysis of Semiconductors

Deep level transient spectroscopy (DLTS) will be the principal technique used in this experiment to evaluate defect concentration levels as well their trap energy and capture cross-sections.

By comparing these characteristics, as well as the annealing behaviour of the defects, to those outlined in literature it is possible to identify the species of defects present in the samples.

DLTS uses the fact that the energy levels of the deep level traps are affected by the energy band bending at the interface between the semiconductor sample and a metal contact. This metal-semiconductor interface forms a Schottky barrier diode. By varying the extent of the band bending by applied biases traps can be filled and emptied. This has an affect on the capacitance of the diode which can be measured and the signal analysed to evaluate the defect concentration and to characterise the defects present. To understand how this is possible it is necessary first to describe the Schottky diode.

3.1 Schottky Barrier Diodes

Schottky diodes can be fabricated on doped semiconductor surfaces to facilitate electrical characterisation of the sample. A Schottky diode is a metal-semiconductor interface that exhibits current rectifying properties. It is similar to a p-n junction diode, except that the Schottky diode characteristics only depend on the majority carrier electrons [9], whereas the p-n diode characteristics depend on both majority and minority carriers.

The diodes fabricated for this lab were first cleaned with solvents to remove any organic contaminates on the surface ('degreasing'). Next the thin 'native' oxide (10-20Å) that exists on the surface of bare silicon is etched off with HF acid and the sample is promptly transferred to thermal evaporator for metal deposition through an Al mask. The evaporation chamber is evacuated to around $5\text{X}10^{-6}$ mbar.

This discussion will focus on the characteristics of a n-type semiconductor Schottky diode. You can get the characteristics of the p-type semiconductor Schottky diode by simple (err..) extension.

The rectification is a result of the Schottky barrier formed at the interface due to the different work functions of the metal (ϕ_m) and semiconductor (ϕ_s). This barrier is characterised by a barrier height (ϕ_b), see fig. 1.

In general the work function of a metal (ϕ_m) is different to a semiconductor and when the two materials come into electrical contact with each other electrons will from the material with the larger Fermi level (or smaller work function) to that with a lower Fermi level.

The work function of a material describes the binding energy of the electrons and is related to their Fermi level (see fig. 1). When the metal and semiconductor come into contact it becomes energetically favourable for electrons in the material with the higher Fermi level to diffuse across to the other material. This builds up a net

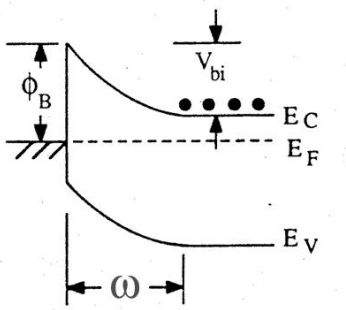

Figure 1: The bending of the energy bands for a n-type semiconductor Schottky barrier diode [12].

charge difference over the interface which creates a built-in voltage (V_{bi}). In n-type silicon if the work function of the metal is larger than that for silicon we get the situation shown in figure 1. The electrons in silicon drift across to the metal and the region left behind will now have a net positive charge and is the depletion region (depleted of majority charge carriers) and characterised by a width (ω). The width of the depletion region can be varied by an applied field (V) and is temperature (T) dependent.

Question 1 *How do V_{bi} and ϕ_b affect the current flow through a Schottky diode?*

Question 2 *What happens if we put a metal with a smaller work function on top of n-type silicon?*

Due to the band bending there is a region in the semiconductor that has been emptied of charge carriers and has a net charge. This is the depletion region characterised by a width ω as seen in figure 1. The depletion region width is given by:

$$\omega = \sqrt{\frac{2\epsilon}{qn}(V_{bi} - (\frac{k_b T}{q}) - V)} \tag{1}$$

Where:
ϵ is the dielectric constant of the semiconductor
n the active dopant concentration in the semiconductor
V_{bi} is the built–in voltage
and V the externally applied bias, as shown in figure 1.

The capacitance of the Schottky diode can be determined by considering the depletion region as a dielectric of width (ω) separating the metal contact of area (A) parallel to the edge of the depletion region in the semiconductor:

$$C = \frac{\epsilon A}{\omega} \tag{2}$$

Substituting equation 1 into 2 we have:

$$C = A\sqrt{\frac{\epsilon q n}{2(V_{bi} - (\frac{k_b T}{q}) - V)}} \tag{3}$$

Armed with this expression, we can measure many properties of the semiconductor by slapping a metal layer on top of the sample (thus forming a Schottky diode) and measuring how the capacitance varies with the applied bias. This is the nub of the C–V and DLTS measurements.

Question 3 *From Equation 3 how can we calculate n and V_{bi} from measured capacitances and applied biases? Check your answer with your demonstrator as you will need to use this later.*

Question 4 *The calculated value for n at a given bias V can be shown to be equal to the uncompensated donor concentration at the edge of the depletion region corresponding the applied bias V [10]. From your answer to question 3 how is it possible to calculate the uncompensated donor concentration n as a function of depth? Check your answer with your demonstrator as you will need to use this later.*

Note that although the 'native' oxide on the surface silicon is etched off some of it may grow back when the samples are being transferred (in air) into the metal deposition chamber. Electrons readily tunnel through this thin oxide layer but there is a small contribution to the barrier height.

3.2 Deep Level Transient Spectroscopy (DLTS)

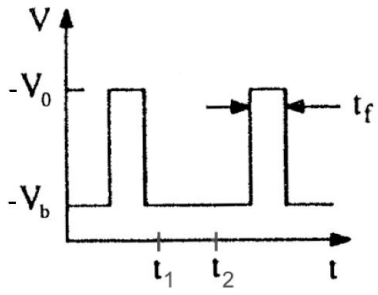

Figure 2: Required pulse cycle for DLTS [12].

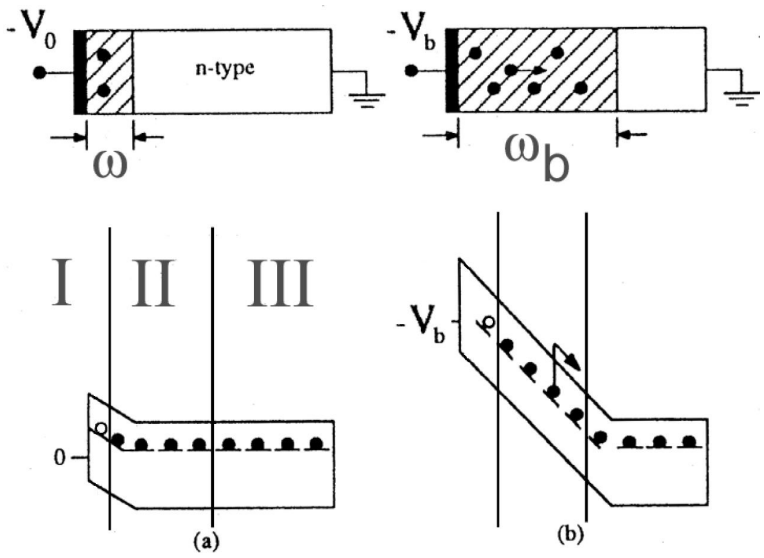

Figure 3: Deep level traps fill and empty depending on the applied bias [12].

DLTS uses a changing bias to fill and empty charge traps to examine the traps over a given depth in the semiconductor. Figure 2 shows an applied bias pulse cycle required for DLTS. Figure 3 shows the effect of

changing the bias on the trap population in the sample. Note also how the depletion region changes.
When the bias voltage is pulsed to the higher V_0 value for some filling pulse time t_p the traps in regions II and III are exponentially filled with electrons from the dopants or conduction band.

Exercise 1 *Write an expression for the concentration of filled traps in region II after the pulse ($n_T(t = 0)$) in terms of t_p, a capture rate r_c and a total trap concentration N_T. Assume all the traps are empty before the pulse and don't forget that there is a finite number of traps to be filled (!).*

The sample however spends most of it's time under a lower bias V_b (stead-state reverse bias) (Fig. 3b) where the traps in region II begin to empty as the band bending makes it energetically favourable for the electrons to spill over into the conduction band of the semiconductor. We call this electron emission from the traps.

The concentration of filled traps in region II after the end of the pulse undergoes an exponential decay that depends on the concentration of filled traps ($n_T(t = 0)$) and the emission rate (e_n).

$$n_T(t) = n_T(t = 0)e^{-e_n t} \tag{4}$$

Now the capacitance is affected by the trapped charge, and the decrease in trapped charge causes an increase in capacitance. This is shown in figure 4 and will be explained in the next section.

The emission rate e_n depends on temperature T, the trap energy level E_T and the capture cross section of the trap σ_c, viz:

$$e_n = \gamma_n \ \sigma_c \ T^2 e^{-(\frac{E_c - E_T}{k_B \ T})} \tag{5}$$

Where γ_n is a set of constants given by:

$$\gamma_n = 2\sqrt{3} M_c (2\pi)^{\frac{3}{2}} k_b^2 m^* h^{-3} \tag{6}$$

Where M_c is the number of minima in the conduction band (6 for silicon) and m^* is the effective electron mass in the conduction band [1]. Since the trap energy level and the capture cross section characterise different defects the emission rate e_n may be different for each defect.

3.2.1 The capacitance transient and DLTS signal

Figure 4 shows how the capacitance of the Schottky diode changes over time as a result of the traps emptying. This capacitance transient can be expressed as:

$$C = C_0 \sqrt{1 - \frac{n_T(t)}{n}} \tag{7}$$

For the case where $n_T << n$ we have:

$$C \approx C_0 (1 - \frac{n_T(t)}{2n}) \tag{8}$$

With DLTS we monitor the change in capacitance over some time interval (measurement or rate window) (t_1, t_2). Where t_1 is the initial delay after the pulse.

The change in capacitance over the rate window is:

$$\delta C = C(t_1) - C(t_2) \tag{9}$$

We divide this by the final capacitance C_0 to form our DLTS signal (S) which can be written as:

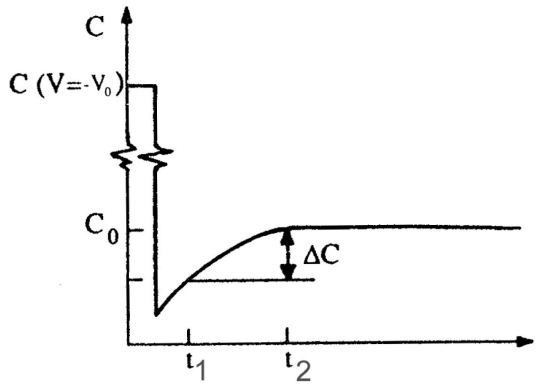

Figure 4: The time variation of capacitance as traps empty [12].

$$S = \frac{\delta\, C}{C_0} = [\frac{n_T}{2n}]\ [e^{-e_n(T)t_2} - e^{-e_n(T)t_1}] \tag{10}$$

where ω_0 and ω_b are the widths of the depletion region under zero and reverse bias respectively.

The bias voltage is pulsed to the higher V_0 value for the filling pulse time t_p to fill the traps again and the cycle is repeated. This allows many readings to be taken to average the signal over.

3.2.2 Calculating trap energy levels and capture cross-sections

Figure 5 shows how the signal changes as a function of temperature when a single trap is present. This occurs due to the temperature dependence of the emission rate and it is the plot of the DLTS signal as a function of temperature that forms a DLTS spectrum.

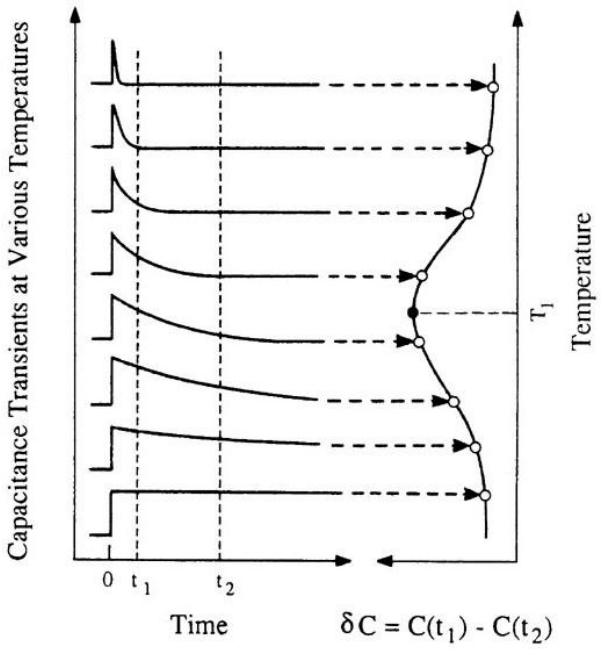

Figure 5: The temperature dependence of the DLTS signal [12].

From equation 10 it is in fact the emission rate that governs what temperature the signal reaches its peak value.

Since this depends on the trap energy (Eq. 5) traps with different energy levels in the band gap will produce a peak at different temperatures.

Exercise 2 *Differentiate Equation 10 with respect to T and show that the emission rate at the temperature that the dlts signal is greatest is given by the following equation:*

$$e_n(T_{peak}) = \frac{ln(\frac{t_2}{t_1})}{t_2 - t_1} \tag{11}$$

N.B. You will NOT NEED to explicitly differentiate e_n, just carry it through.

Equation 11 shows that the measurement times t_1 and t_2 set what is known as a rate window for the emission rate. It can be shown that different rate windows cause the peak to shift in temperature. By taking DLTS spectra at various rate windows we may obtain a range of values for the peak temperature associated with each emission rate and hence each defect. Using these values and noting that at the peak temperature the emission rate is given by your answer to Equation 11 it is possibe to calculate both the trap energy level and the capture cross-section.

Question 5 *Re-arrange Equation 5 to obtain $ln(\frac{e_n}{T^2})$ in terms of $\frac{1}{T}$.*

Since the temperature at which the DLTS signal peaks changes with the emission rate window we can generate a plot of the above equation for various temperatures and emission rates. A plot of a temperature dependant rate against $\frac{1}{T}$ is known as an Arhhenius plot.

How can this be used to calculate the trap energy and capture cross section? Again check with your demonstrator as this will be important later in the DLTS analysis.

3.2.3 Calculating trap concentrations

Note that in equation 10, if the trap concentration n_T is zero then the signal is also zero. This is to say that the magnitude of the DLTS signal is also proportional to the concentration of defects present, n_T, and can be expressed as:

$$\left.\frac{\delta\, C}{C_0}\right|_{max} = \frac{n_T}{2n}\frac{1-r}{r^{\frac{r}{r-1}}} \tag{12}$$

Where $r = \frac{t_2}{t_1}$. We can then write for the trap concentration:

$$n_T = 2\left.\frac{\delta\, C}{C_0}\right|_{max} n\frac{r^{\frac{r}{r-1}}}{1-r} \tag{13}$$

Note that the trap concentration is dependant on electrically active dopant concentration in the region that is being probed. This is determined with C-V measurements and is outlined in that section.

Exercise 3 *Derive equation 12.*

3.3 Deep-level traps in implanted silicon

(You will also find a good introduction to ion implantation in Streetman [2].)

It has been well established that ion implantation introduces many defects into the substrate [3, 4, 5]. In particular Frenkel defects are created which consist of a host atom that has been knocked off its substitutional lattice site into an interstitial position (i.e. between crystal lattice sites) leaving a vacancy behind in the lattice [5]. At room temperature the vacancy and interstitial can migrate and separate without recombination. This occurs for 4-10% of the Frenkel defects created during ion implantation [5]. These defects can go on to cluster together or form stable defect complexes with impurities. About 10-25% of the Frenkel defects that survive recombination form a di-vacancy cluster [6] which is a characteristic defect for ion implanted silicon [3, 7].

The defects of prime importance for electrical devices are those that are electrically active, meaning that they can trap charge carriers in the device. Electrically active traps are basically unoccupied states in the band-gap of a semiconductor that trap charge carriers. This occurs mostly due to defects having dangling bonds which are unpaired electrons, and the traps exist at some energy level depending on the structure of the defect. Identification of defect structures and atomic constituents is achieved most reliably with Electron Para-magnetic Resonance (EPR) measurements although not every defect complex has an EPR signature. The identity of defects which do not show up in EPR are often inferred from detailed analysis of their annealing characteristics.

In the case of ion-implanted phosphorus doped silicon the interstitial silicon does not form a trap, but the vacancies can migrate and combine with impurities such as oxygen and carbon (found in even top grade commercially available silicon wafers) as well as with the phosphorus dopant to form vacancy complexes. Chemical cleaning of the silicon can also lead to incorporation of hydrogen which is believed to be the constituent of many defect complexes.

Defects can be characterised by their position in the band-gap of a semiconductor relative to the conduction band (trap energy, E_t), and their cross-section for trapping (capture cross-section, σ). The values reported for electron traps in ion-implanted silicon are found in table 1. This table shows the average value for the trap energies found in the literature. Absolute errors in the last digit are shown in parentheses, no error is quoted for occasions where there is only one reference for the defect, nor is the error quoted for capture cross-sections that have an error that is over an order of magnitude difference. V indicates vacancy, other letters indicate elements, subscripts 2 & 3 indicate the number of vacancies in a cluster and superscripts indicate the charge state of the trap. Other subscripts indicate either substitutional or interstitial atomic positions in the lattice.

4 Experimental Work

The SULA DLTS system and its associated electronics is a joint MARC group/Part 3 laboratory apparatus and is thus also used for research. The research of the MARC group (and perhaps even one of your demonstrators) depends on the correct functionality of the equipment so it is especially important to treat it with respect.

A rough experimental outline is as follows:

- Do C-V measurements on a n-Si Schottky diode at room temp and 79K
- Analyse data to determine active dopant concentration and barrier height
- Do DLTS and C-T measurements on a ion implanted or irradiated Si sample.
- If time permits, do one of the following:
  - Examine samples implanted/irradiated under different conditions
  - Perform quasi-isothermal DLTS with different biases and analyse data to determine depth profile of the defect. Involves more complicated calculations.

Defect type	Trap Energy [ev]	Capture cross–section [cm^2]
H–related	0.10	–
H–related	0.13	–
HC	0.15(1)	–
VO	0.17(1)	$7(4)x10^{-15}$
C_sC_i	0.17(0)	$8x10^{-18}$
V–related	0.19(1)	$3.5x10^{-17}$
V_2^{2-}	0.22(1)	$5(4)x10^{-16}$
V_2O	0.27	–
V_3O	0.30	–
VO-H, other H–related	0.30(2)	$3x10^{-15}$
V–related	0.35(1)	$5x10^{-16}$
H–related	0.39(1)	$1x10^{-17}$
H–related	0.41(1)	–
VP_s	0.42(2)	$5(3)x^{-15}$
V_2^-	0.42(1)	$5(3)x^{-15}$
H–related	0.45(1)	$1x10^{-17}$
V_2–related	0.47	–
H–related	0.50(1)	–
Unknown	0.59	–

Table 1: Defect characteristics as published in the literature for defects relevant to ion-implanted n-type silicon.

The equipment consists of three bunches of stuff; the racks of electronics, the computer stuff and the cryostat. Most of the components aren't cheap off the shelf items so treat them with respect. Furthermore, the DLTS system is also used for reseach by the MARC/COE in the school. If you're curious about the research work talk to your demonstrator.

4.1 The racks of electronics

The box at the top sitting on the PC is the temperature controller. This is primarily under the 'remote' control of the PC and software. Do not play with it, if there is an error message or other problem consult your demonstrator.

Next comes the digital CRO for monitoring the appled bias on the sample.

Then there is the SULA DLTS electronics. Further information on these units can be found in the SULA DLTS user manual.

Underneath this is a rack of BNC connectors. Computers don't come with BNC sockets, so this rack is purely to interface the PC with all the electronics.

The last tray at the bottom is the variac for the diaphragm pump (for adjusting the pump speed) and the thermocouple vacuum gauge for the roughing line pressure (see section 4.3).

4.2 The computer stuff

The experiment is primarily controlled by a labview program, which has a nice GUI into which you can enter the values that you would like certain parameters to assume. For example, to change the sample temperature, just type (say) 275 into the relevant box, hit [Idle at initial temp], and the electronics will do the rest.

Your demonstrator will take you through most of what you need to do, but a few extra hints will be provided here. For example, you need to tell the software what scale the capacitance meter is set to so that the correct capacitance value is recorded.

You will be analysing the data using a command-line plotting/analysis software called genplot, which has some similarities to IDL and C (for those who are into such stuff). You will be using pre-written programs (macros) to analyse the data you have taken using Labview (using ASCII files). Your demonstrator will show you how to do this.

4.3 The cryostat and sample holder

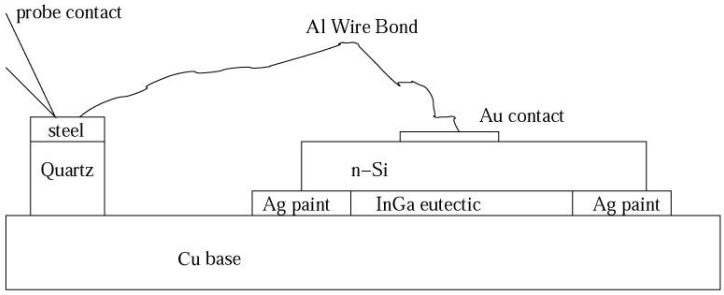

Figure 6: Sample holder schematic

Ask your demonstrator to loas a sample and to show you how the sample is connected and how the temperature is controlled and measured inside the chamber.

The sample mounting setup is shown in figure 6. The InGa is a 'eutectic' which is liquid at room temperature. We use it because it forms an Ohmic contact with the sample (unlike the gold contact on top, which forms a Schottky contact). The silver paint is there to hold the sample in place. The quartz is an insulator to stop current from flowing between the probe contact and the backing plate, bypassing the sample.

Question 6 *What property of In or Ga makes InGa a suitable Ohmic contact? What about the Ag? [Hint: It has nothing to do with resistivity/conductivity]*

The sample is electrically isolated from the chamber in order to minimise stray capacitance. For the same reason, the coaxial cables connecting the sample to the electronics are kept as short as possible.

The sample needs to be cooled in order to minimise the thermally generated currents which act as noise in the measurement. We need precise and accurate control of the temperature in order to do some of the funky temp-dependent stuff later. For this reason the stage is fitted with a heater and two thermocouples (electric thermometers). Thermocouple A is used for temperature control and is situated at the base of the 'Cu cold head' in the chamber near the heater, Thermocouple B is situated at the top of the cold head near the sample and is taken as the measured sample temperature.

The cooling is provided by drawing liquid nitrogen up the tube at the bottom and through a tube around the base of (and in intimate thermal contact with) the cold head and out the side, through the transparent plastic tube. This is acheived by pumping on the transparent plastic tube with a diaphragm pump (the same as used for fish tanks). Note that liquid nitrogen is in fact very difficult to pump and in fact the pump doesn't actually pump on liquid nitrogen as it evaporates before reaching it.

This diaphragm/N_2 pump is controlled by a variable voltage source (variac-this one is red and lives under the electronics). 70 V is good for cooling down to 77 K (takes about 15 mins); 20 V will keep it there.

Beware of liquid nitrogen-it is cold. It also displaces air upon evaporation, so if you keep the doors closed and

fill the room with nitrogen, you may faint or suffocate. Ensure that you have read the safety manual before proceeding, don't mess with the liquid nitrogen, and keep the doors open!

The sample chamber is also evacuated using a rotary roughing pump. It is kept under vacuum for a couple of reasons. It keeps out any moisture, oils and dust in the air which may contaminate the sample and sample chamber. Most importantly it is needed for thermal isolation of the cold head so that lower temperatures can be maintained. The pump is connected to the chamber via a power off venting valve which closes off the port to the tee-piece (hence chamber) and vents the roughing line (the line connected to the pump) when the pump is switched off. This is to prevent 'suck back' of oil from the pump when it is off.

4.4 Making a room temperature C-V measurement

The C-V measurement will allow us to determine the barrier height, depletion width and active dopant density of the sample.

Equipment:

- Air Liquide LN_2 cryostat/dewar (rotary roughing pump, N_2 diaphram pump, temp controller)
- National instruments BNC-adaptor/DAC, SULA/Labview software
- SULA Pulse generator and capacitance meter units

The bias is applied to the top diode contact of sample via the output BNC connection on the [Pulse generator] unit (Labelled as _-_) and the capacitance is read from the back contact which is connected to the [In] of the [Capacitance meter] unit.

EVACUATING THE SAMPLE CHAMBER

1. Connect the Pulse generator output [_-_] to the [Probe A] coax of the cryostat.
2. Connect the [Back contact] to the [In] of the [Capacitance meter]
3. The black buttons on the Capacitance meter control what is displayed on the LED. C shows the capacitance divided by whatever [Crange] is set to (e.g. Crange is 300 pF and the reading is 0.50 then the capacitance is 150 pF). The reading should always be positive and less than about 1.3, if it isn't contact your demonstrator or change the Crange.
4. To maintain a stable temperature for measurement the cryostat is simultaneously heated and cooled with liquid nitrogen. Before you proceed you need to evacuate the chamber to 300-400 mTorr with the roughing pump to remove as much air, and in particular any water vapour in the air, as possible.
5. Open the chamber valve, close the venting valve **being careful not to overtighten the valve as this will damage the bellows inside**
6. Disconnect the tube connecting the venting valve to the dewar, this allows the pressure build up in the dewar to escape
7. Turn on the [Vac. Gauge] via the bottom power board
8. Turn on the [Roughing pump] via the power board and note down in the log book how long it takes to reach the operating pressure (below 400 mTorr). Then switch it off but leave the Vac. Gauge on and make sure it reaches the blue line (true atm. pressure). If it doesn't contact your demonstrator.
9. Typically the output of the pulse generator is tee'd off to the CRO so that the applied bias can be observed. The applied DC bias can be controlled in two ways, with the [Offset] knob and via an input into the [Ext. Bias] connection. The software will use the digital to analogue converter (DAC) in the PC to apply a DC analogue bias to the sample via this input from [DACOUT0] of the BNC adaptor
10. Connect the [Ext. bias] to the [DACOUT0] BNC of the NI BNC adaptor.

11. For starters perform a C-V measurement at room temperature biasing the diode over as large a range as possible. Click on [i] on the [Capacitance meter] to read the leakage current in the diode in μA. Adjust the [offset] reverse DC bias applied to the diode to determine the voltage range over which the leakage is less than 5 μA. Do not read off the voltage from the dial as it is not accurate.

12. Set [Offset] bias on the [Pulse generator] to 0

13. This completes the hardware setup and the rest of the setup is via the SULA software.

14. A voltage interval of around 0.2 V will be needed for a nice resolution data set for analysis. To correct for stray background capacitance from the wires and sample chamber the software needs to subtract this off the raw capacitance reading, this has been measured for various capacitance range settings and appears in table 2.

15. Flip the [Experiment] type to C-V

16. Set the [Initial temp] to something around room temp, turn on the diaphragm pump and set the voltage to around 10 V, record the length of time and voltage you have this on in the logbook.

17. Click [Idle at initial temp] to set the temperature controller.

18. Set [Initial bias] and [Final bias] to the minimum and maximum biases you previously determined.

19. The [Stray capacitance] is given in table 2

20. Set the [Background capacitance] to [Use current value]

21. The [Crange] should be set to be the same as the capacitance meter setting

22. The [Preamp gain] is irrelevant (I think)

23. Click [Run experiment] to start the measurement. N.B. The measurement will not start until the temperature of thermocouple A is at the setpoint.

Crange (pF)	Background Capacitance (pF)
100	5.40
300	5.26
1000	5.09

Table 2: Table of Stray/Background Capacitances for Cu mounting plate and AirLiquide cyrostat

4.5 Making a low temperature C-V measurement

The chamber should still be under vacuum and inserted into the dewar at this stage. If not, make it so. It is important to ensure the chamber is at the correct low vacuum otherwise it will water vapour will condense in the chamber and it will take a long time to pump down to a low temperature.

COOLING THE SAMPLE/COLD HEAD

1. Ensure that the chamber is within the operating pressure (less than 400 mTorr). Record the chamber pressure and how long it took to pump down in the user log book

2. The chamber valve should be closed and roughing pump turned off to reduce any electrical noise and vibrations.

3. Set the [Initial Temp.] to around 79 K now and click [Idle at Initial temp.]

4. The Spoint on the temp. controller should now be at this value.

5. Ensure that the venting tube between the venting valve and the dewar collar is disconnected to allow N_2 build up in the dewar to escape.

6. Turn on the power for the N_2 diaphram pump and increase the voltage to 70 V. The sample should now be cooling, record how long it takes to cool down in the user log book. It should take approximately 15 minutes to reach 79 K. If it doesn't contact your demonstrator. Since the pump is quite loud, you may wish to leave the room at this stage.

7. Once you have reached the initial temperature reduce the diaphram pump voltage to 10-20 V and make sure that the temperature controller can maintain a stable temperature (within +/- 0.5 K). Now repeat the C-V measurement.

4.6 Analysing the C-V data

4.6.1 Determine the built-in voltage of the diode

You will need to re-examine your answers to exercise 3 and question 3. You should only fit the data over biases close to zero. This is because will find that the active dopant concentration is not uniform over depth. Furthermore you should not calculate values for each data point and it is much more accurate to perform a linear fit.

The SULA labview program can be used to calculate the built in voltage but you also be able to calculate this yourself.

4.6.2 Calculate the barrier height

Calculate the barrier height which can be expressed as:

$$\phi_b = V_{bi} + E_f \tag{14}$$

Where E_f is the position of the Fermi level relative to the conduction band and is given by:

$$E_f = \frac{k_b T}{q} Log_e[\frac{n_c}{n}] \tag{15}$$

n_c is the Density of states in the conduction band of silicon:

$$n_c = 2 \times 10^6 (2\pi m^* \frac{k_b T}{h^2})^{\frac{3}{2}} \tag{16}$$

N.B. Your answer should be expressed in eV and greater than the built–in voltage but less than the band gap of silicon.

Now that you have the built-in voltage and the barrier height, sketch a labeled band diagram for the diode.

4.6.3 Calculate the active dopant concentration

Calculate this as a function of depth for both of your scans. You will need to re-examine your answers to exercise 3 and question 3 and convert the capacitance to a corresponding depletion width (depth). You will need these results for analysing the DLTS data.

You can use Excel for data analysis but export tab delimited two column data and use the Genplot macro diffdat.mac provided to differentiate it.

1. First copy diffdat.mac to the same directory your data file is in.

2. Open the [XGenplot] program and change to the directory where your data is

3. Then type [xeq diffdat.mac] to execute the differentiation macro

Genplot commands you may find useful are:

[pwd] -lists current directory

[ls] or [dir] -lists contents of directory

[cd xxx] -changes to directory xxx

[cd ..] -goes up a directory level

[read] -reads your data file

[show] -show the data

[pl] -plot the data

[trans dy/dx] -differentiates the data

[write] -saves data file to disk

[fit lin] -to perform a linear fit

[lt n] -to plot with a line type n

[lt 0 sy n] -to plot with symbol type n

[pen n] -to plot with colour n

[ov -fit] -to overlay the fit

You can now import the file into Excel to calculate the free carrier concentration. You should obtain values on the order of 10^{15} cm^{-3}. Comment on any differences between your scans.

From your profile determine a depth range over which you want to perform DLTS over and establish what biases are needed for depletion depths over this range. Discuss this with your demonstrator before continuing.

4.7 DLTS measurement

Equipment:

- Air Liquide LN_2 cryostat/dewar (rotary roughing pump, N_2 diaphram pump, temp controller)
- National instruments BNC-adaptor/DAC, SULA/Labview software
- SULA Pulse generator, capacitance meter, 4 correlator units

Again the chamber should still be under vacuum and inserted into the dewar. Furthermore the sample should be at 78 K. If not, make it so.

1. Setting up the filling pulse and correlators. The electronics can now be setup for a DLTS measurement. The first thing to do is set the [Offset] on the [Pulse generator] to place the diode under reverse bias. This should be set so that the depletion region is at the end of range you decided in the previous section. Monitor the voltage with the [V] setting on the [Capacitance meter]. Since the bias output of the pulse generator should also be connected to the CRO you should also be able to observe this on the CRO. To ensure proper operation check the leakage current by pressing the [i] setting on the [Capacitance meter]. The reading is in μA, it should not be more than 5 μA.

2. Set [Offset] on the [Pulse generator] to the value you have determined above as read on the [V] setting on the [Capacitance meter]

3. Check the leakage current by pressing the [i] setting on the [Capacitance meter], reading is is uA. Reduce bias if reading is more than 5 μA reduce the reverse bias

4. Next turn on the pulse generator with the [On/Off] toggle switch. Press the [_-_] button on the [Capacitance meter]. The display now indicates the voltage at which the bias is pulsed to. Set the pulse [Amplitude] on the pulse generator so that the depletion width will be at the start of the region of uniform free carriers. You should be able to now see the pulse on the CRO. If not, ensure that the CRO is set to the DC mode and external trigger. If the trigger is set to normal you may need to adjust the trigger level.

5. Set [Amplitude] on the [Pulse generator] to the bias reading as determined avove as read on the [_-_] setting on the [Capacitance meter]

6. The pulse [Width] needs to be set to fill as many traps as possible. The pulse width affects how many of the defects will be filled during the pulse since they have a characteristic capture cross-section (and hence capture rate). For the defects in ion implanted silicon this needs to be between 10 and 100 ms. The electronics does not monitor this and the CRO needs to be used. Although a larger pulse fills more defects it also means that it will take longer for the electronics to recover after a pulse. The filling of defects also does not scale linearly with pulse width but has an inverse exponential behaviour so it is often not necessary to use a long pulse.

7. Set pulse [Width] and the range knob below it to between 10 and 100 ms as read seen in the applied bias on the CRO.

8. The [Initial delay] (t_1) of the correlators need to be set to examine the capacitance transient over the correct rate windows. There are four correlators so we can simultaneously look at four different rate windows. The correlators work so that the rate window is equal to 4.3xt_1 (i.e. t_2=5.3xt_1). For ion implanted silicon we need values of $t_1 < 5$ ms. Correlator 1 should have the largest initial delay with the next correlator having consecutively smaller initial delays. The [Y] outputs of the correlators should now also be connected to the corresponding channels of the NI BNC-adaptor (Channels 1, 2, 3, 4).

9. Set [Initial delay] for each correlator to be less than 5 ms, where Correlator 1 having the largest value and each consecutive correlator having consecutively smaller values.

10. Ensure the [Y] outputs of the correlators are connected to the corresponding channels of the NI BNC-adaptor (Ch1, 2, 3, 4).

11. The [Period] of pulse repetition needs to be carefully set to ensure the electronics have enough time to recover. Follow the rules:

    - Period > [Width] + 10*[Initial Delay on all correlators]
    - Period < 200*[Initial Delay on correlators 1 and 2]

12. The pulse generator is now setup for DLTS and the rest of the measurement electronics can be set up.

13. The [Pre-amp] output on correlator 1 unit should be connected to the CRO to monitor the capacitance signal of the diode that is fed into the correlators for measurement. Increase the [Pre-amp gain] on the correlator to as large as possible without producing a noisy signal. The pre-amp output should now be connected to the [Input] of the auxiliary correlators (3 and 4).

14. Connect the [Pre-amp] output on correlator 1 to the CRO

15. Increase the [Pre-amp gain] on the correlator to as large as possible without producing a noisy signal on the 1 V/div scale.

16. Connect the [Pre-amp] output to the [Input] of the auxiliary correlators (3 and 4).

17. The [TC] value of the correlators affects how fast the internal capacitors discharge and hence how fast consecutive measurements can be made. TC contributes to the total time constant TC_{tot} which should be less than 12 ms and as close as possible for each correlator. TC_{tot} depends on many factors and has been calculated for you. Refer to the table on the wall of the lab.

18. Set [TC] so that TC_{tot} is as close as possible for each correlator according to the table on the wall in the lab.

19. The hardware is now setup and the rest of the experiment is controlled by the software. Change the front panel [Experiment] to [DLTS] and enter all the hardware settings into the window. The [Initial Temp.] should be set to 78 K and the [Final Temp.] to room temperature. The mode should be on [Step]. The stray capacitance is irrelevant and the [Offset] should be set to [measure at start]. The offset measurement is important because it removes any offsets from the correlator readings so that if there are no defects (hence no change in capacitance) the signal will be zero.

20. Change [Experiment] to [DLTS] on SULA software front panel.

21. Enter all the hardware settings into the window.

22. Set the [Initial Temp.] to 78 K, the [Final Temp.] to room temperature, and the mode to [Step].

Offset should be set to [measure at start].

23. Once you have completed this you can click [Run experiment] and the scan will take approximately 1-2 hours to complete.

4.8 Perfoming a C-T measurement

You will need to know C_o at various temperatures to determine the defect concentrations (Eq. 13). You can do this on a case by case basis or perform a scan over the whole temperature range used in DLTS.

4.9 Analysing the DLTS data

4.9.1 Calculate the defect concentrations

Calculate the defect concentration for each of the defect peaks observed.

4.9.2 Characterise the defects observed

Use the SULA analysis program to determine the peak DLTS signal temperatures for each of the defects. You should not rely on the program to calculate E_t and σ_c however since it will not give you any useful imformation on how good the linear fit is. Therefore use Excel or genplot. N.B. A good fit gives R^2 close to 1 or χ^2 close to 0.

Important constants:
Diameter of diode = 780 μm with an uncertainty of 20 μm
q= 1.60218E-19 /* electron charge [C]
eps0= 8.85418E-14 /* permittivity of free space [F/cm]
epss= 11.9 /* Dielectric constant for Si
kb= 1.38066E-23 /* Boltzmann's constant [J/K]
h= 6.62617E-34 /* Planck's constant [J.s]
me0= 9.1095E-31 /* electron rest mass [kg]
me= $(0.98 \text{x} 0.19^2)^{1/3}$ /* effective electron mass factor in Si at 300K

4.10 If time permits..

...it won't. :-)

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Acknowledgements

These notes were written by Matthew Lay in 2004, and tweaked by David Hoxley in the same year. Samples were prepared and mounted by Matthew Lay with wire bonding done by Sean Hearne.